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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,143	02/17/2004	Alexander L. Barr	SC13265TP	2254

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EXAMINER	
COLEMAN, WILLIAM D	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/780,143	BARR ET AL.	
	Examiner	**Art Unit**	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 06 January 2006.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-13 and 15-24 is/are rejected.

7)☒ Claim(s) 14 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed January 6, 2006 have been fully considered but they are not persuasive.

2. Applicants contend that neither Ieong et al., U.S. Patent 6,815,278 B1 herein known as Ieong and Yamazaki et al., U.S. Patent 6,803,264 B2 herein known as Yamazaki fail to teach the limitations of independent claims 7 and 15, there is further added the requirement of "pre" which makes reference to the semiconductor layer being strained prior to the claimed step of bonding.

3. In response to Applicants contention that neither Ieong nor Yamazaki teaches the limitation of "pre" which makes reference to the semiconductor layer being strained prior to the claimed bonding step, please note that the carrier wafer 12 in Ieong can be silicon or silicon germanium prior to the formation of the additional layers. It is well known that carrier wafer 12 would be "pre-strained" (i.e., prior to straining is relaxed) and therefore carrier wafer 12 is relaxed prior to being strained when bonded as seen in FIG. 2 of Ieong, therefore Applicants argument is moot.

4. Applicants contend that they have not been able to find any such corresponding semiconductor layer in either Yamazaki or Ieong that is strained.

5. In response to Applicants contention that neither Ieong nor Yamazaki contains a strained layer please see column 2, line 55 of Ieong where Ieong teaches a strained silicon layer and the

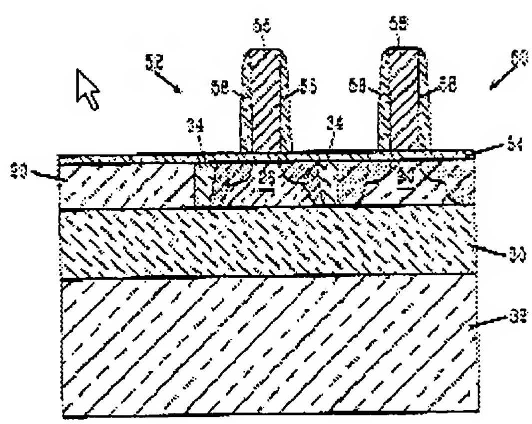
silicon germanium layer is relaxed. In Yamazaki, the strained layer is inherently disclosed because Yamazaki discloses the SMART-CUT process and wafer-bonding (please see column 3, lines 37-47). It is well known that bonding silicon and silicon germanium results in strained features in the substrate. The Examiner has provide several references to support this well known feature between silicon and silicon germanium.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Ieong et al., U.S. Patent 6,815,278 B1.



8. Pertaining to claim 1, Ieong teaches a method for forming a semiconductor device comprising:

providing a semiconductor substrate **32**;

forming an insulating layer on a surface of the semiconductor substrate **30**;

providing a strained semiconductor layer on the insulating layer **20**;

defining a <100> direction of the strained semiconductor layer (see column 1, lines 21-49); and

forming a transistor on the strained semiconductor layer, wherein the transistor is aligned along the < 100> direction of the strained semiconductor layer.

9. Pertaining to claim 2, Ieong teaches the method of claim 1, wherein the strained semiconductor layer is in a tensile stress state (it is well known that when thin layers of silicon are joined to silicon-germanium stress is produced).

10. Pertaining to claim 3, Ieong teaches the method of claim 1, wherein providing a strained semiconductor layer further comprises:

providing an at least partially relaxed silicon-germanium layer on the insulating layer; and

forming a silicon layer on the at least partially relaxed silicon-germanium layer to form the strained semiconductor layer (because Ieong teaches that one can vary the thickness of both the silicon-germanium layer and the silicon layer, it is well known that the variations and thickness of the layers will result in stress and relaxation of the claimed films).

11. Pertaining to claim 4, Ieong teaches the method of claim 1, wherein providing a strained semiconductor layer on the insulating layer comprises:

forming a semiconductor layer on the insulating layer; and

straining the semiconductor layer (it is well known that providing very thin layers of silicon will result in a strained layer).

12. Pertaining to claim 5, Ieong teaches the method of claim 1, further comprising defining a <110> direction of the semiconductor substrate (Ieong teaches the importance of the crystal orientation for high mobility of both p-type and n-type MOSFETs in column 1, lines 21-49).

13. Pertaining to claim 6, Ieong teaches the method of claim 5, further comprising aligning the <110> direction with the <100> (the motivation of this rejection is found in the rejection of claims 1 and 5 above).

14. Pertaining to claim 7, Ieong teaches a method for forming a semiconductor device comprising:

providing a semiconductor substrate **32**;

defining a <110> direction of the semiconductor substrate **32**;

forming an insulating layer **30** on a surface of the semiconductor substrate;

providing a pre-strained semiconductor layer **20**;

defining a <100> direction of the pre-strained semiconductor layer **20**;

bonding the semiconductor layer to the insulating layer, wherein the < 100> of the pre-strained semiconductor layer is aligned with the <110> direction of the semiconductor substrate; and

forming a transistor on the pre-strained semiconductor layer, wherein the transistor is aligned along the <100> direction of the pre-strained semiconductor layer.

15. Pertaining to claim 8, Ieong teaches the method of claim 7, wherein providing a pre-strained semiconductor layer further comprises:

providing an at least partially relaxed silicon-germanium layer; and

forming a silicon layer on the at least partially relaxed silicon-germanium layer form the pre-strained semiconductor layer (because Ieong teaches that the thickness can be varied, this limitation is met).

16. Pertaining to claim 9, Ieong teaches the method of claim 7, wherein the semiconductor device is

characterized as being a silicon-on-insulator device.

17. Pertaining to claim 10, Ieong teaches the method of claim 7, wherein bonding of the pre-strained semiconductor layer to the insulating layer is performed by thermal wafer bonding (column 5, lines 18-19).

18. Pertaining to claim 11, Ieong teaches the method of claim 7, wherein forming a transistor on the pre-strained semiconductor layer comprises aligning a source/drain axis of the transistor along the <100> direction of the pre-strained semiconductor layer.

19. Pertaining to claim 12, Ieong teaches the method of claim 7, wherein forming a transistor on the pre-strained semiconductor layer comprises aligning a source/drain axis of the transistor perpendicular to the <100> direction of the pre-strained semiconductor layer.

20. Pertaining to claim 13, Ieong teaches the method of claim 7, further comprising cleaving the semiconductor device through the pre-strained semiconductor layer.

21. Pertaining to claim 15, Ieong teaches a method for forming a semiconductor device comprising:

providing a semiconductor substrate; defining a crystal orientation of the semiconductor substrate;

forming an insulating layer on a surface of the semiconductor substrate;

providing a pre-strained semiconductor layer; defining a crystal orientation of the pre-strained semiconductor layer;

bonding the pre-strained semiconductor layer to the insulating layer, wherein the crystal orientation of the pre-strained semiconductor layer is not aligned with the crystal orientation of the semiconductor substrate; and

forming a transistor on the pre-strained semiconductor layer, wherein a source/drain axis of the transistor is aligned along the crystal orientation of the pre-strained semiconductor layer.

22. Pertaining to claim 16, Ieong teaches the method of claim 15, wherein the crystal orientation of the pre-strained semiconductor layer is determined to enhance current transport capability of a PMOS transistor.

23. Pertaining to claim 17, Ieong teaches the method of claim 15, wherein the semiconductor device is a silicon-on-insulator device.

24. Pertaining to claim 18, Ieong teaches the method of claim 15, wherein providing a pre-strained semiconductor layer further comprises:

providing an at least partially relaxed silicon-germanium layer; and forming a silicon layer on the at least partially relaxed silicon-germanium layer form the pre-strained semiconductor layer.

25. Pertaining to claim 19, Ieong teaches the method of claim 15, wherein defining a crystal orientation of the semiconductor substrate comprises defining a <110> direction of the semiconductor substrate.

26. Pertaining to claim 20, Ieong teaches the method of claim 15, wherein defining a crystal orientation of the pre-strained semiconductor layer comprises defining a <100> direction of the pre-strained semiconductor layer.

27. Pertaining to claim 21, Ieong teaches the method of claim 20, wherein forming a transistor on the pre-strained semiconductor layer comprises aligning a source/drain axis of the transistor along the <100> direction of the pre-strained semiconductor layer.

28. Pertaining to claim 22, Ieong teaches the method of claim 21, wherein forming a transistor on the pre-strained semiconductor layer comprises aligning a source/drain axis of the transistor perpendicular to the <100> direction of the pre-strained semiconductor layer.

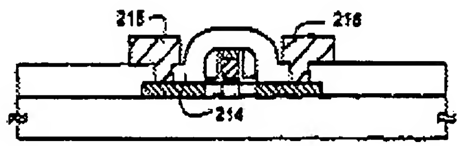
29. Pertaining to claim 23, Ieong teaches the method of claim 15, further comprising cleaving the semiconductor device through the pre-strained semiconductor layer.

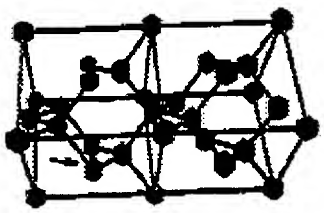
30. Pertaining to claim 24, Ieong teaches the method of claim 15, further comprising polishing the pre-strained semiconductor layer after cleaving (the Examiner takes the position that it is well known to provide a CMP after a wiring/metallization process).

31. Please note that the Examiner provides an additional art rejection to show how well known the claimed invention has been disclosed.

32. Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al., U.S. Patent 6,803,264 B2.

Yamazaki discloses a semiconductor process as claimed. See FIGS. 1A-9B, where Yamazaki teaches the following limitations.





33. Pertaining to claim 1, Yamazaki teaches a method for forming a semiconductor device comprising:

providing a semiconductor substrate **101**;

forming an insulating layer on a surface of the semiconductor substrate **102**;

providing a strained semiconductor layer on the insulating layer;

defining a <100> direction of the strained semiconductor layer; and

forming a transistor on the strained semiconductor layer, wherein the transistor is aligned along the < 100> direction of the strained semiconductor layer.

34. Pertaining to claim 2, Yamazaki teaches the method of claim 1, wherein the strained semiconductor layer is in a tensile stress state.

35. Pertaining to claim 3, Yamazaki teaches the method of claim 1, wherein providing a strained semiconductor layer further comprises:

providing an at least partially relaxed silicon-germanium layer on the insulating layer; and

forming a silicon layer on the at least partially relaxed silicon-germanium layer to form the strained semiconductor layer.

36. Pertaining to claim 4, Yamazaki teaches the method of claim 1, wherein providing a strained semiconductor layer on the insulating layer comprises:

forming a semiconductor layer on the insulating layer; and

straining the semiconductor layer.

37. Pertaining to claim 5, Yamazaki teaches the method of claim 1, further comprising defining a <110> direction of the semiconductor substrate.

38. Pertaining to claim 6, Yamazaki teaches the method of claim 5, further comprising aligning the <110> direction with the <100>.

39. Pertaining to claim 7, Yamazaki teaches a method for forming a semiconductor device comprising:

providing a semiconductor substrate;

defining a <110> direction of the semiconductor substrate;

forming an insulating layer on a surface of the semiconductor substrate;

providing a pre-strained semiconductor layer; defining a <100> direction of the pre-strained semiconductor layer; bonding the semiconductor layer to the insulating layer, wherein the

< 100> of the pre-strained semiconductor layer is aligned with the <110> direction of the semiconductor substrate; and forming a transistor on the pre-strained semiconductor layer, wherein the transistor is aligned along the <100> direction of the pre-strained semiconductor layer.

40. Pertaining to claim 8, Yamazaki teaches the method of claim 7, wherein providing a pre-strained semiconductor layer further comprises:

providing an at least partially relaxed silicon-germanium layer; and

forming a silicon layer on the at least partially relaxed silicon-germanium layer form the pre-strained semiconductor layer.

41. Pertaining to claim 9, Yamazaki teaches the method of claim 7, wherein the semiconductor device is characterized as being a silicon-on-insulator device.

42. Pertaining to claim 10, Yamazaki teaches the method of claim 7, wherein bonding of the pre-strained semiconductor layer to the insulating layer is performed by thermal wafer bonding.

43. Pertaining to claim 11, Yamazaki teaches the method of claim 7, wherein forming a transistor on the pre-strained semiconductor layer comprises aligning a source/drain axis of the transistor along the <100> direction of the pre-strained semiconductor layer.

44. Pertaining to claim 12, Yamazaki teaches the method of claim 7, wherein forming a transistor on the pre-strained semiconductor layer comprises aligning a source/drain axis of the transistor perpendicular to the <100> direction of the pre-strained semiconductor layer.

45. Pertaining to claim 13, Yamazaki teaches the method of claim 7, further comprising cleaving the semiconductor device through the pre-strained semiconductor layer.

46. Pertaining to claim 15, Yamazaki teaches a method for forming a semiconductor device comprising:

providing a semiconductor substrate;

defining a crystal orientation of the semiconductor substrate;

forming an insulating layer on a surface of the semiconductor substrate;

providing a pre-strained semiconductor layer;

defining a crystal orientation of the pre-strained semiconductor layer;

bonding the pre-strained semiconductor layer to the insulating layer, wherein the crystal orientation of the pre-strained semiconductor layer is not aligned with the crystal orientation of the semiconductor substrate; and forming a transistor on the pre-strained semiconductor layer, wherein a source/drain axis of the transistor is aligned along the crystal orientation of the pre-strained semiconductor layer.

47. Pertaining to claim 16, Yamazaki teaches the method of claim 15, wherein the crystal orientation of the pre-strained semiconductor layer is determined to enhance current transport capability of a PMOS transistor.

48. Pertaining to claim 17, Yamazaki teaches the method of claim 15, wherein the semiconductor device is a silicon-on-insulator device.

49. Pertaining to claim 18, Yamazaki teaches the method of claim 15, wherein providing a pre-strained semiconductor layer further comprises:

providing an at least partially relaxed silicon-germanium layer; and

forming a silicon layer on the at least partially relaxed silicon-germanium layer form the pre-strained semiconductor layer.

50. Pertaining to claim 19, Yamazaki teaches the method of claim 15, wherein defining a crystal orientation of the semiconductor substrate comprises defining a <110> direction of the semiconductor substrate.

51. Pertaining to claim 20, Yamazaki teaches the method of claim 15, wherein defining a crystal orientation of the pre-strained semiconductor layer comprises defining a <100> direction of the pre-strained semiconductor layer.

52. Pertaining to claim 21, Yamazaki teaches the method of claim 20, wherein forming a transistor on the pre-strained semiconductor layer comprises aligning a source/drain axis of the transistor along the <100> direction of the pre-strained semiconductor layer.

53. Pertaining to claim 22, Yamazaki teaches the method of claim 21, wherein forming a transistor on the pre-strained semiconductor layer comprises aligning a source/drain axis of the transistor perpendicular to the <100> direction of the pre-strained semiconductor layer.

54. Pertaining to claim 23, Yamazaki teaches the method of claim 15, further comprising cleaving the semiconductor device through the pre-strained semiconductor layer.

55. Pertaining to claim 24, Yamazaki teaches the method of claim 15, further comprising polishing the pre-strained semiconductor layer after cleaving.

Objections

56. Claim 14 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

57. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

58. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

59. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

60. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

61. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

W. David Coleman
Primary Examiner
Art Unit 2823

WDC